19-0220; Rev 3; 10/03

Serial Controlled, 8-Channel SPST Switch

General Description

The MAX335 analog switch with serial digital interface offers eight separately controlled single-pole-single-throw (SPST) switches. All switches conduct equally in either direction, and on-resistance (100Ω) is constant over the analog signal range.

These CMOS switches can operate continuously with power supplies ranging from ±4.5V to ±20V and handle rail-to-rail analog signals. Upon power-up, all switches are off, and the internal serial and parallel shift registers are reset to zero. The MAX335 is equivalent to two DG211 quad switches but controlled by a serial interface.

The interface is compatible with the Motorola SPI interface standard. Functioning as a shift register, this serial interface allows data (at DIN) to be locked in synchronous with the rising edge of clock (SCLK). The shift register's output (DOUT) enables several MAX335s to be daisy chained.

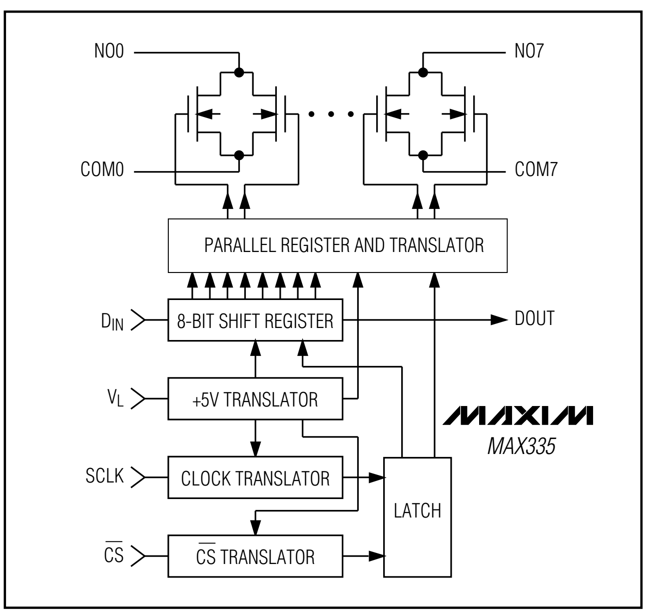
Applications

Serial Data Acquisition and Process Control

Avionics

Signal Routing

Networking



Features

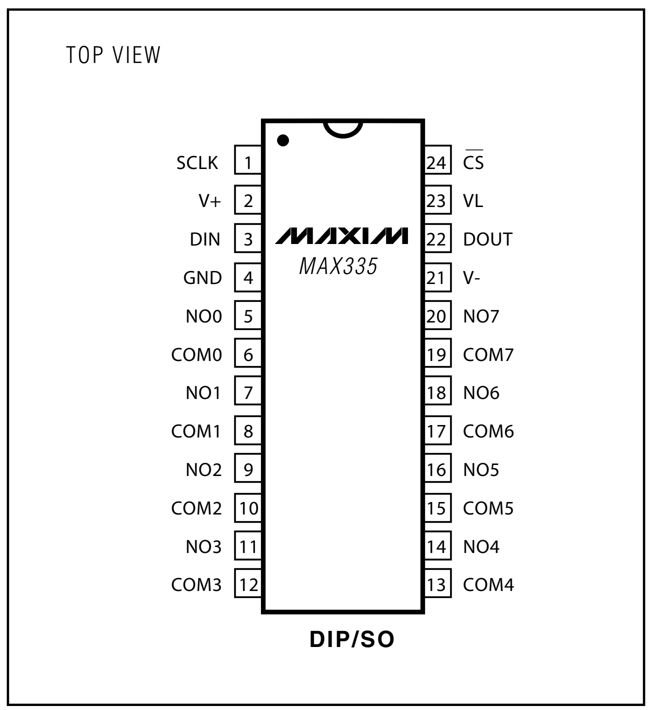
- ♦ 8 Separately Controlled SPST Switches
- ♦ SPI-Compatible Serial Interface
- ♦ Accepts ±15V Analog Swings
- ♦ Multiple Devices Can Be Daisy Chained

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX335CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX335CWG	0°C to +70°C	24 Wide SO
MAX335C/D	0°C to +70°C	Dice*
MAX335ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX335EUG	-40°C to +85°C	24 TSSOP
MAX335EWG	-40°C to +85°C	24 Wide SO
MAX335MRG	-55°C to +125°C	24 Narrow CERDIP**

Contact factory for dice specifications.
*** Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-
- V+ 44V
- GND 25V
- V_L ....(GND - 0.3V) to (V+ + 0.3V)
- SCLK, $\overline{CS}$, DIN, DOUT, NO_, COM_ ....V- -2V to V+ +2V or 30mA, whichever occurs first

Continuous Current (any terminal) 30mA
Peak Current, NO or COM (pulsed at 1ms, 10% duty cycle MAX)..............................00mA

Note 1: All leads are soldered or welded to PC boards.

Continuous Power Dissipation (T_A = +70°C) (Note 1)
- Narrow Plastic DIP (derate 13.33mW/°C above +70°C)1067mW
- Wide SO (derate 11.76mW/°C above +70°C).................941mW

Narrow CERDIP (derate 12.50mW/°C above +70°C) 1000mW
TSSOP (derate 12.2mW/°C above +70°C)..........................30mA
Operating Temperature Ranges
MAX335C_ _ ....0°C to +70°C
MAX335E_ _ ....-40°C to +85°C
MAX335MRG..-55°C to +125°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10sec)..............................+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_L = +5V ±10%, V+ = 15V, V- = -15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	T_A = T_{MIN} to T_{MAX}		-15		15	V
On-Resistance	R_{ON}	V_{COM} = ±10V, I_{NO} = 1mA	T_A = +25°C		100	150	Ω
						200	
NO Off-Leakage Current	$I_{NO(OFF)}$	V_{COM} = -14V, V_{NO} = +14V	T_A = +25°C	-1	0.002	1	nA
				-20		20	
		V_{COM} = -14V, V_{NO} = +14V	T_A = +25°C	-1	0.002	1	
				-20		20	
COM Off-Leakage Current	$I_{COM(OFF)}$	V_{COM} = -14V, V_{NO} = +14V	T_A = +25°C	-1	0.002	1	nA
				-20		20	
		V_{COM} = -14V, V_{NO} = +14V	T_A = +25°C	-1	0.002	1	
				-20		20	
COM On-Leakage Current	$I_{COM(ON)}$	V_{COM} = V_{NO} = +14V	T_A = +25°C	-2	0.01	2	nA
				-40		40	
		V_{COM} = V_{NO} = -14V	T_A = +25°C	-2	0.01	2	
				-40		40	
DIGITAL I/O							
DIN, SCLK, $\overline{CS}$ Input Logic Threshold High	V_{IH}	V_L = +5V		2.4			V
		V_L = +15V		11			
DIN, SCLK, $\overline{CS}$ Input Logic Threshold Low	V_{IL}	V_L = +5V				0.8	V
		V_L = +15V				3	
DIN, SCLK, $\overline{CS}$ Input Current Logic High	I_{INH}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 2.4V		-1	0.03	1	µA
		V_L = +15V, V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 11V		-1	0.03	1	
DIN, SCLK, $\overline{CS}$ Input Current Logic Low	I_{INL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V		-1	0.03	1	µA
		V_L = +15V, V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 3V		-1	0.03	1	
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = 0.8mA		3.5		V_L	V

ELECTRICAL CHARACTERISTICS (continued)

(V_L = +5V ±10%, V+ = 15V, V- = -15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL I/O							
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = -1.6mA				0.4	V
V_L RESET Voltage	V_{LL}	(Note 2)		0.8			V
V_L RESET Voltage	V_{LH}		T_A = +25°C			2.4	V
SCLK Input Hysteresis	$SCLK_{HYST}$		T_A = +25°C		100		mV
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$	T_A = +25°C		200	400	ns
						500	
Turn-Off Time	t_{OFF}	From rising edge of $\overline{CS}$	T_A = +25°C		90	400	ns
						500	
NO Off-Capacitance	$C_{NO(OFF)}$	V_S = GND, f = 1MHz	T_A = +25°C		2		pF
COM Off-Capacitance	$C_{COM(OFF)}$	V_D = GND, f = 1MHz	T_A = +25°C		2		pF
Channel On-Capacitance	$C_{COM(ON)}$	V_D = V_S = GND, f = 1MHz	T_A = +25°C		8		pF
Off Isolation	OIRR	R_L = 100Ω, C_L = 15pF, V_S = $1V_{RMS}$, f = 100kHz	T_A = +25°C		90		dB
Channel-to-Channel Crosstalk	CCRR	R_L = 50Ω, C_L = 15pF, V_S = $1V_{RMS}$, f = 100kHz	T_A = +25°C		100		dB
Break-Before-Make Delay	T_{BBM}			25	15		ns
Clock Feedthrough at S, D (Note 3)	ESCLK	D_{LOAD} = S_{LOAD} = 75Ω, measured at S and D	T_A = +25°C			100	nV-sec
POWER SUPPLIES							
Power-Supply Voltage Range	V+/V-			±4.5		±20	V
V_L Power-Supply Voltage Range	V_L			4.5		V+	V
V+ Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V/5V	T_A = +25°C		150	300	µA
						500	
V- Supply Current	I-	DIN = $\overline{CS}$ = SCLK = 0V/5V	T_A = +25°C		0.01	10	µA
						10	
V_L Supply Current	I_L	DIN = $\overline{CS}$ = SCLK = 0V/5V	T_A = +25°C		50	100	µA
						200	

Note 2: When V_L falls below this voltage, all switches are set off and the internal shift register is cleared (all zero).
Note 3: Guaranteed, not production tested.

TIMING CHARACTERISTICS OF SERIAL DIGITAL INTERFACE (Figure 1)

(V_L = +5V ±10%, V+ = +15V, V- = -15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

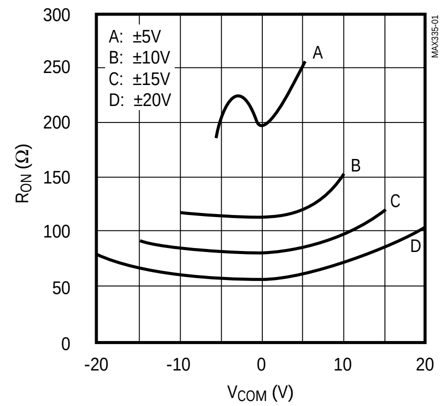
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SCLK Maximum Frequency	f_{SCLK}			2.1			MHz
Cycle Time	$t_{CH} + t_{CL}$			480			ns
$\overline{CS}$ Lead Time	t_{CSS}			240			ns
$\overline{CS}$ Lag Time	t_{CSH2}			240			ns
SCLK High Time	t_{CH}			190			ns
SCLK Low Time	t_{CL}			190			ns
Data-Setup Time	t_{DS}			200			ns
Data-Hold Time	t_{DH}			0			ns
DOUT Data Valid After Falling SCLK	t_{DO}	50% of SCLK to 10% of DOUT CL = 10pF	T_A = +25°C		240		ns
						400	
DOUT Data-Hold Time After Rising SCLK (Note 4)		C_L = 10pF		0			ns
Rise Time of DOUT (Note 3)		20% V_L to 70% V_L, C_L = 10pF				100	ns
Allowable Rise Time at DIN, SCLK, $\overline{CS}$ (Note 3)		20% V_L to 70% V_L, C_L = 10pF				2	µs
Fall Time of DOUT (Note 3)		70% V_L to 20% V_L, C_L = 10pF				100	ns
Allowable Fall Time at DIN, SCLK, $\overline{CS}$ (Note 3)		70% V_L to 20% V_L, C_L = 10pF				2	µs

Note 4: This specification guarantees that data at D_{OUT} never appears before SCLK's falling edge.

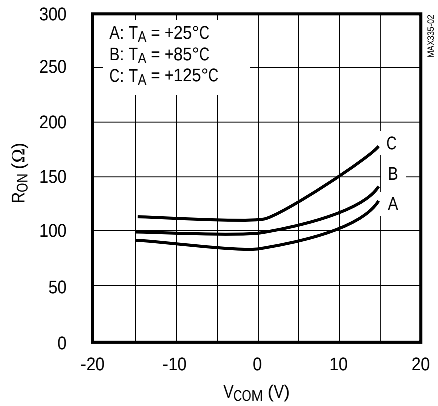
Typical Operating Characteristics

(V+ = +15V, V- = -15V, V_L= 5V, T_A = +25°C, unless otherwise noted.)

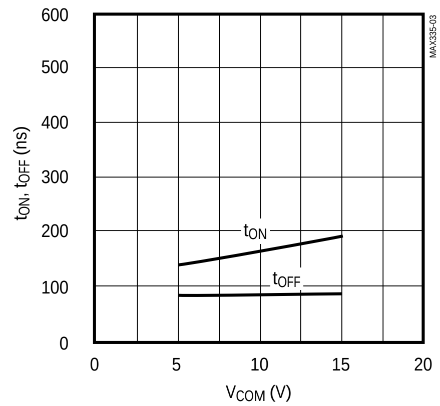
R_{ON} vs. V_{COM} AND POWER-SUPPLY VOLTAGE



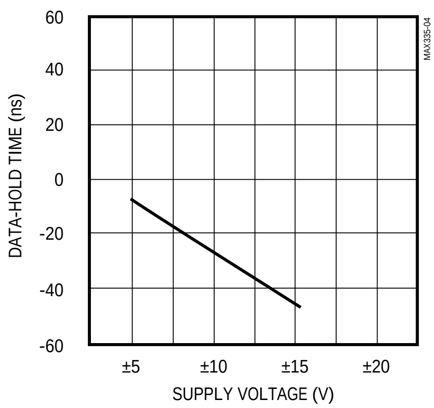
R_{ON} vs. V_{COM} AND TEMPERATURE



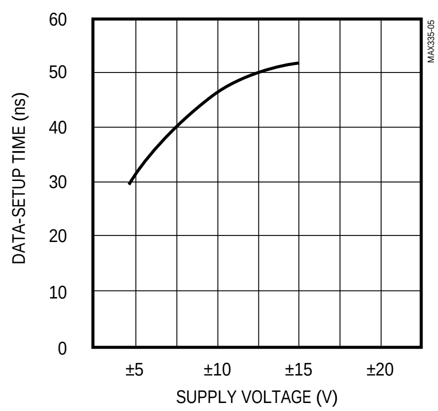
t_{ON}, t_{OFF} vs. V_{COM}



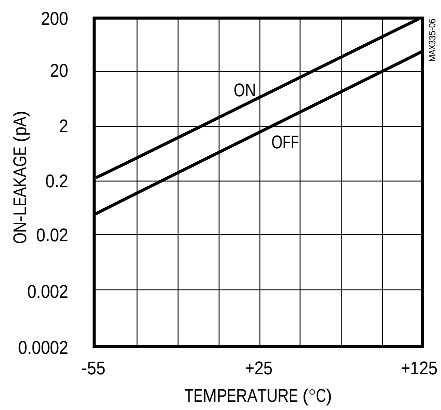
DATA-HOLD TIME vs. POWER-SUPPLY VOLTAGE



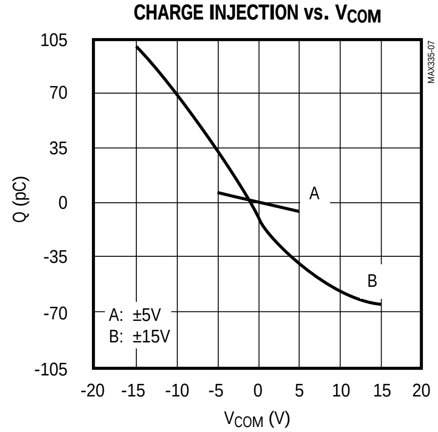
DATA-SETUP TIME vs. POWER SUPPLY



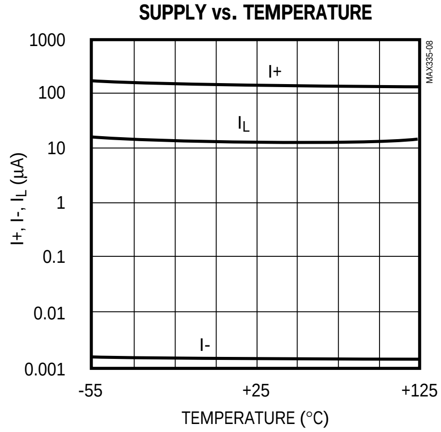
LEAKAGE CURRENT vs. TEMPERATURE



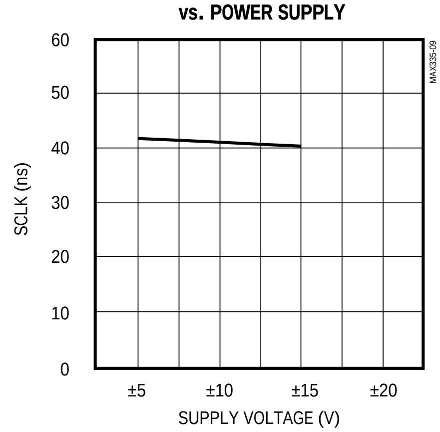
CHARGE INJECTION vs. V_{COM}



SUPPLY vs. TEMPERATURE



MINIMUM SCLK PULSE WIDTH vs. POWER SUPPLY



Pin Description

PIN	NAME	FUNCTION
1	SCLK	Serial Clock Input
2	V+	Positive Supply Voltage
3	DIN	Serial Data Input
4	GND	Ground
5	NOØ	Switch 0
6	COMØ	Switch 0
7	NO1	Switch 1
8	COM1	Switch 1
9	NO2	Switch 2
10	COM2	Switch 2
11	NO3	Switch 3
12	COM3	Switch 3
13	COM4	Switch 4
14	NO4	Switch 4
15	COM5	Switch 5
16	NO5	Switch 5
17	COM6	Switch 6
18	NO6	Switch 6
19	COM7	Switch 7
20	NO7	Switch 7
21	V-	Negative Supply Voltage
22	DOUT	Serial Data Output
23	V_L	Logic Supply/Reset
24	$\overline{CS}$	Chip Select

Detailed Description

Serial Digital Interface

Basic Operation

Refer to Figure 2. The MAX335 interface can be thought of as an 8-bit shift register controlled by $\overline{CS}$. While $\overline{CS}$ is low, input data appearing at DIN is clocked into the shift register synchronous with SCLK's rising edge. The data is an 8-bit word, each bit controlling one of eight switches in the MAX335 (Table 1). DOUT is the output of the shift register, with data appearing synchronous with SCLK's falling edge. Data at DOUT is simply the input data delayed by eight clock cycles.

When shifting the input data, D7 is the first bit in and out of the shift register. While shifting data, the switches remain in their original configuration. When the 8 bits of data have been shifted in, $\overline{CS}$ is brought high. This updates the new switch configuration and inhibits further data from entering the shift register. Transitions at DIN and SCLK have no effect when $\overline{CS}$ is high, and DOUT holds the last bit in the shift register.

The MAX335 three-wire serial interface is compatible with the SPI™ and Microwire™ standards. If interfacing with a Motorola processor serial interface, set CPOL = 0. The MAX335 is considered a slave device (Figures 2 and 3). Upon power-up, the shift register contains all zeros, and all switches are off.

The latch that drives the analog switch is only updated on the rising edge of $\overline{CS}$ when SCLK is low. If SCLK is high when $\overline{CS}$ rises, the latch will not be updated until SCLK goes low. The CPOL = 1, CPHA = 1 SPI configuration does not update the latch correctly.

Daisy Chaining

For a simple interface using several MAX335s, "daisy chain" the shift registers as shown in Figure 5. The $\overline{CS}$ pins of all devices are connected together, and a stream of data is shifted through the MAX335s in series. When $\overline{CS}$ is brought high, all switches are updated simultaneously. Additional shift registers may be included anywhere in series with the MAX335 data chain.

Addressable Serial Interface

When several serial devices are configured as slaves, addressable by the processor, DIN pins of each MAX335 are connected together (Figure 6). Address decode logic individually controls $\overline{CS}$ of each slave device. When a slave is selected, its $\overline{CS}$ is brought low, data is shifted in, and $\overline{CS}$ is brought high to latch the data. Typically, only one slave is addressed at a time. DOUT is not used.

Digital Feedthrough

Digital feedthrough energy measures 100nV-sec, which means that with no filtering at the signal channel, feedthrough from a sharply rising clock edge into an unfiltered switch channel can be measured at 1Vp-p for 100ns. However, even 100pF capacitance in the switch channel, when combined with the switch resistance, yields a filter that reduces this transient to 10mVp-p typical. To reduce digital feedthrough, hysteresis (150mV typ) was added to the SCLK input so triangle or sine waves may be used.

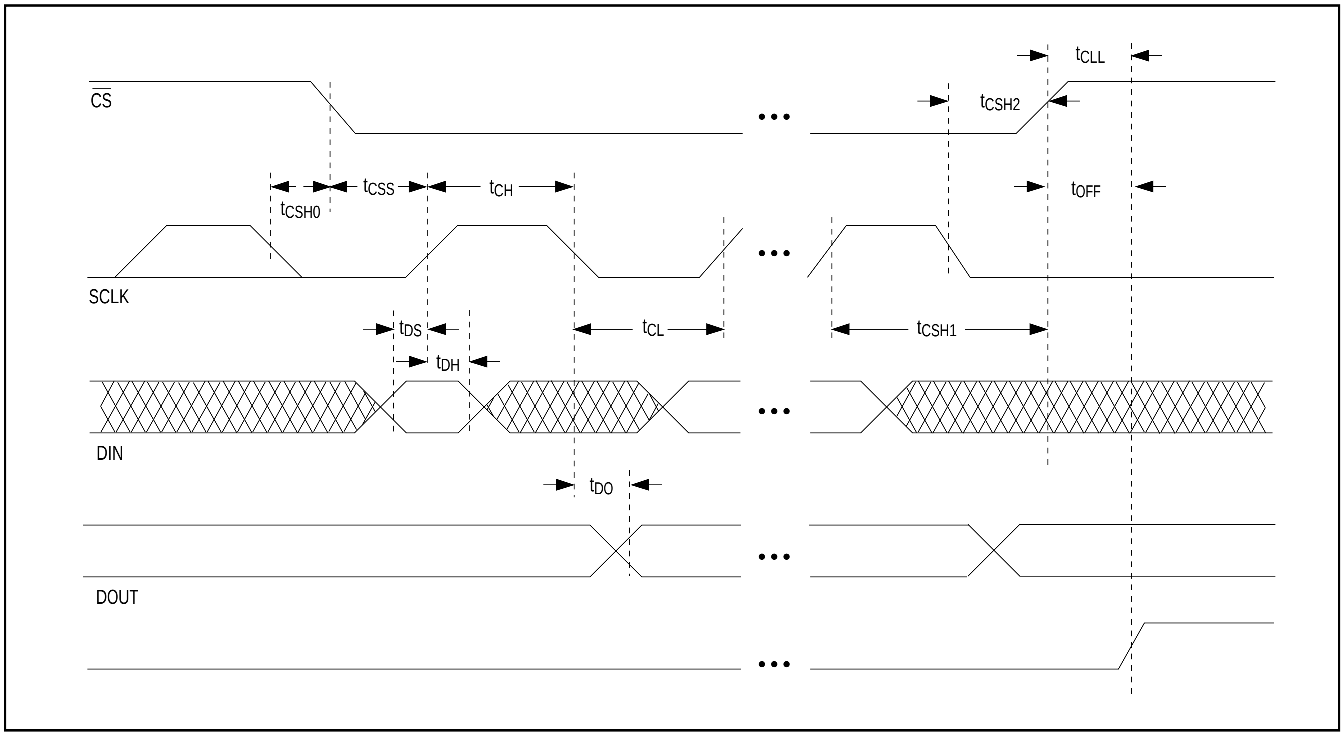


Figure 1. Timing Diagram

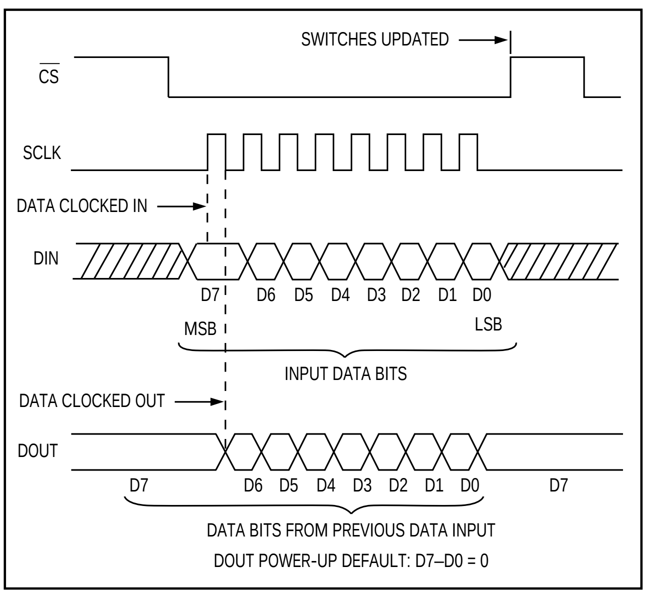


Figure 2. Three-Wire Interface Timing

Table 1. Serial-Interface Switch Programming

DATA BITS								FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	Switch 7 open (off)
1	X	X	X	X	X	X	X	Switch 7 closed (on)
X	0	X	X	X	X	X	X	Switch 6 open
X	1	X	X	X	X	X	X	Switch 6 closed
X	X	0	X	X	X	X	X	Switch 5 open
X	X	1	X	X	X	X	X	Switch 5 closed
X	X	X	0	X	X	X	X	Switch 4 open
X	X	X	1	X	X	X	X	Switch 4 closed
X	X	X	X	0	X	X	X	Switch 3 open
X	X	X	X	1	X	X	X	Switch 3 closed
X	X	X	X	X	0	X	X	Switch 2 open
X	X	X	X	X	1	X	X	Switch 2 closed
X	X	X	X	X	X	0	X	Switch 1 open
X	X	X	X	X	X	1	X	Switch 1 closed
X	X	X	X	X	X	X	0	Switch 0 open
X	X	X	X	X	X	X	1	Switch 0 closed

X = Don't care

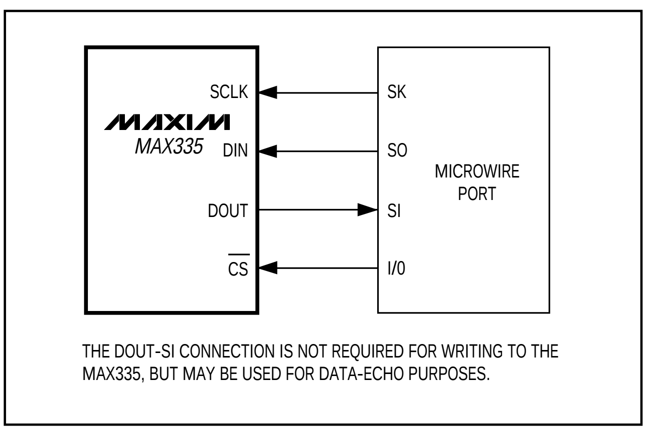


Figure 3. Connections for Microwire

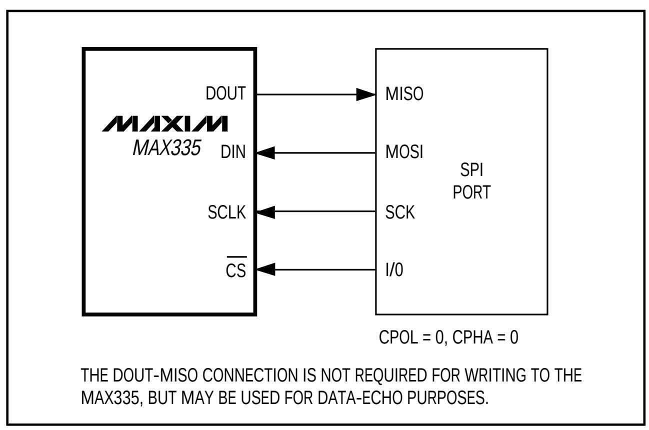


Figure 4. Connections for SPI

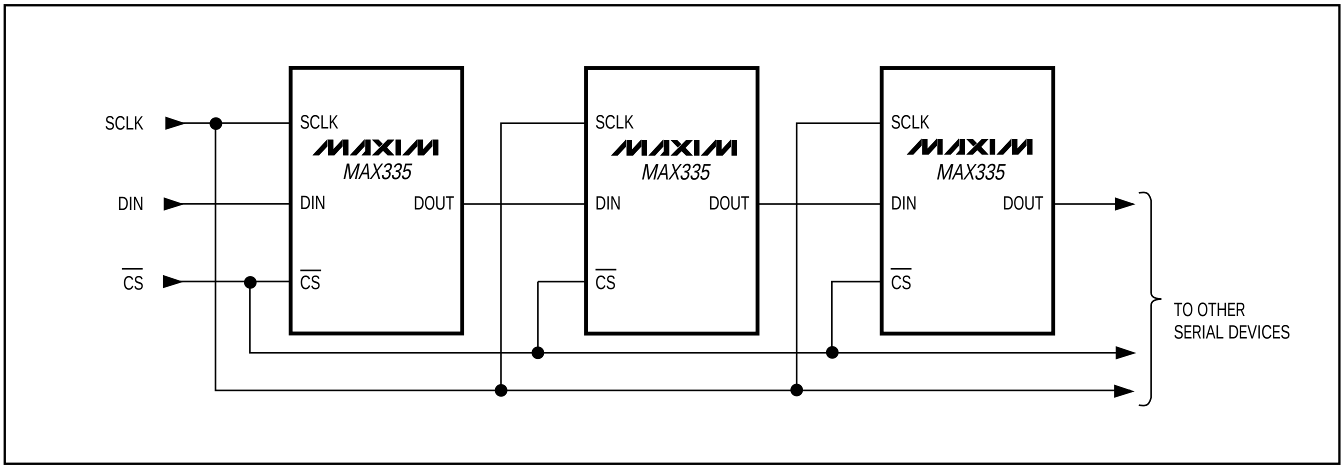


Figure 5. Daisy-Chained Connection

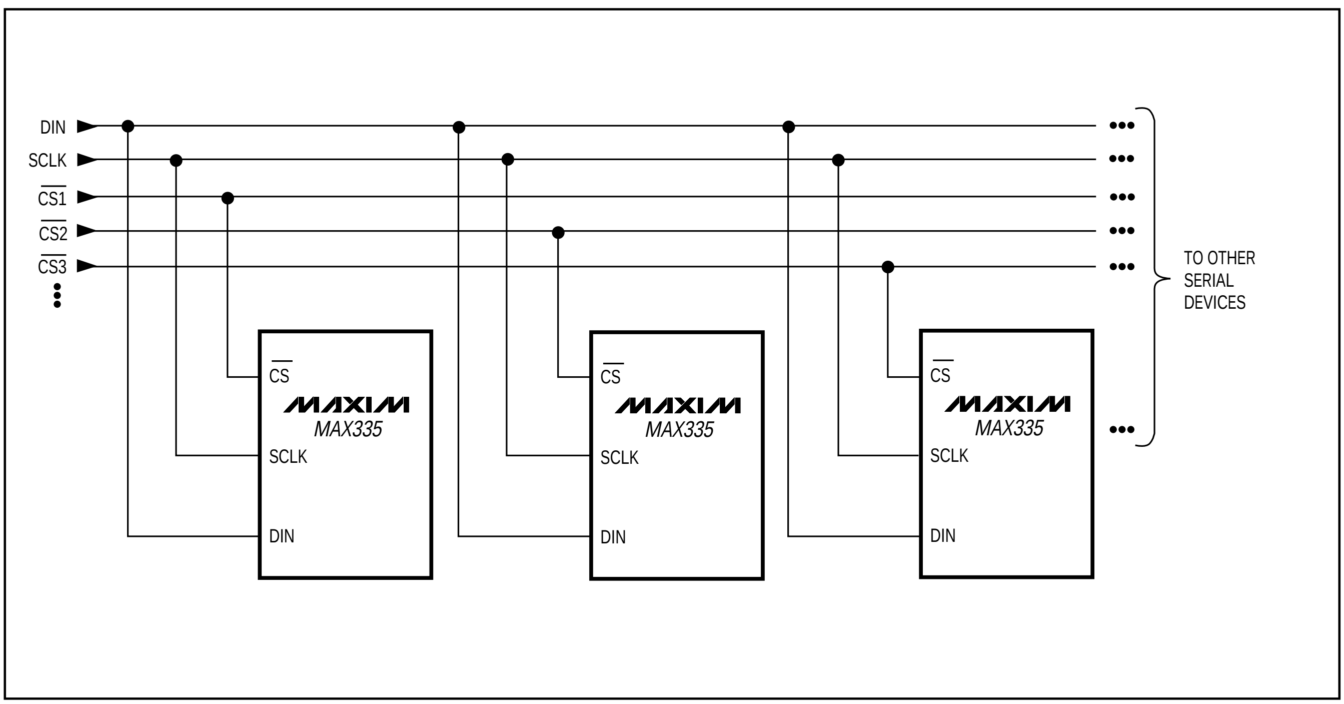


Figure 6. Addressable Serial Interface

Serial Controlled, 8-Channel SPST Switch

Applications Information

8 x 1 Multiplexer

To use the MAX335 as an 8 x 1 multiplexer, tie all drains together (COM0 to COM7); the mux inputs now source each switch (NO0 to NO7). Input a single 0V to +3V pulse at DIN. As this is clocked through the register by SCLK, each switch will sequence on one at a time.

4-2 Differential Multiplexer

To use the MAX335 as a 4-2 differential multiplexer, tie COM0 through COM3 together and COM4 through COM7 together. Differential inputs will be the source inputs as follows: (NO0, NO4), (NO1, NO5), (NO2, NO6), (NO3, NO7). Figure 7 shows the serial input control at DIN required to turn on two switches making a differential multiplexer.

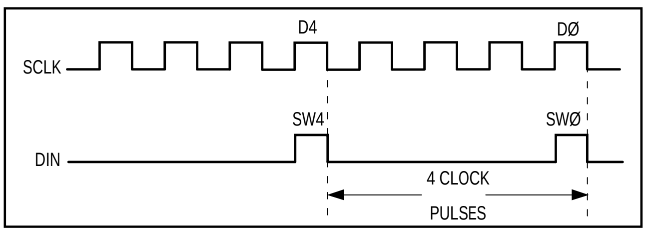


Figure 7. Differential Multiplexer Input Control

$\overline{CS}$ is held low for four clock pulses; the first pulse is clocked into the fifth switch position as the second pulse is clocked into the first switch position. $\overline{CS}$ is pulled high to update switches; then $\overline{CS}$ is pulled low, and SCLK advances pulses to S1 and S5 positions, where $\overline{CS}$ is pulled high to update, etc.

SPDT Switches

Tie COM0 to NO1 so that NO0 and COM1 are now inputs and COM0/NO1 is the common output. SP is common output. Up to four SPDT switches can be made from each MAX335. Multiples of four or more can be made by daisy chaining devices. In Figure 8, DIN is a pulse train. Again, $\overline{CS}$ is held low to clock in pulses and $\overline{CS}$ is pulled high to update; $\overline{CS}$ is held low to shift pulses, then pulled high to update, etc.

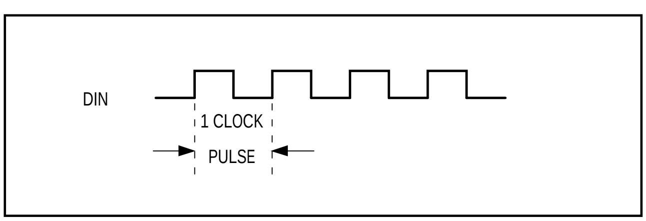


Figure 8. Serial-Input Control for SPDT Switch

Reset Function

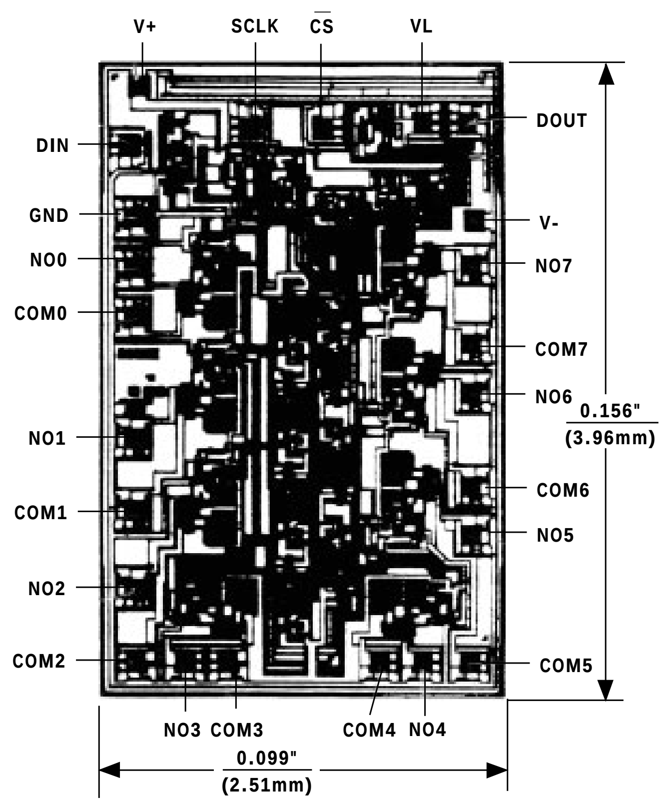
Pulsing V_L below +0.8V initiates the power-up reset function. The switches are set to the off position, and the serial shift register is reset to all zeros.

Power-Supply Operation

The MAX335 operates with V = ±4.5V to ±20V and V_L = +5V. With V- tied to ground, the part operates with V+ = +10V to +30V.

The V_L supply sets TTL input compatibility at a 1.6V switching threshold. As V_L is raised, the switching threshold is raised, so the part is no longer TTL compatible. The MAX335 also operates with a single power supply: V_L = V+ and V- = 0V. With V_L tied to V+, the V_L supply cannot be used as a reset function.

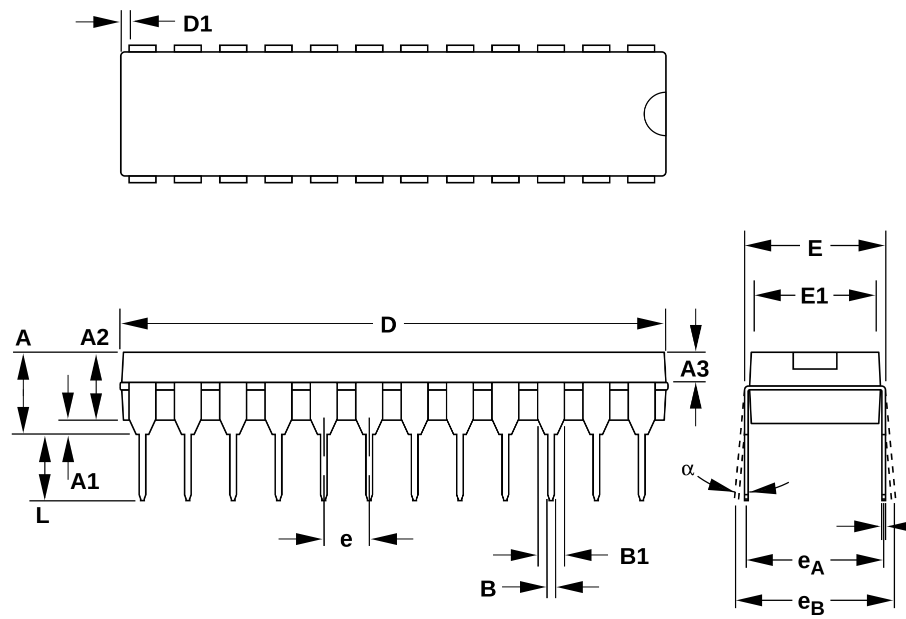
Chip Topography



TRANSISTOR COUNT: 387

SUBSTRATE CONNECTED TO V+.

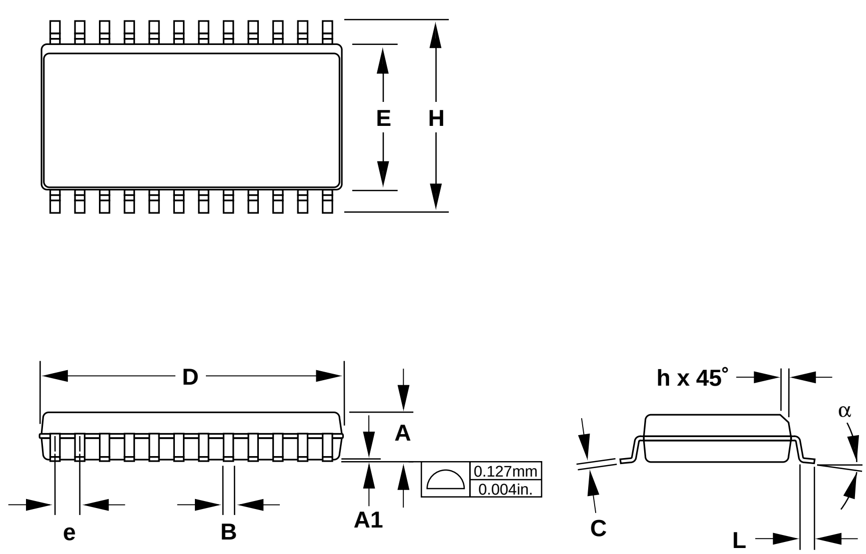
Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	1.235	1.265	31.37	32.13
D1	0.050	0.080	1.27	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

21-337A

24-PIN PLASTIC DUAL-IN-LINE (NARROW) PACKAGE



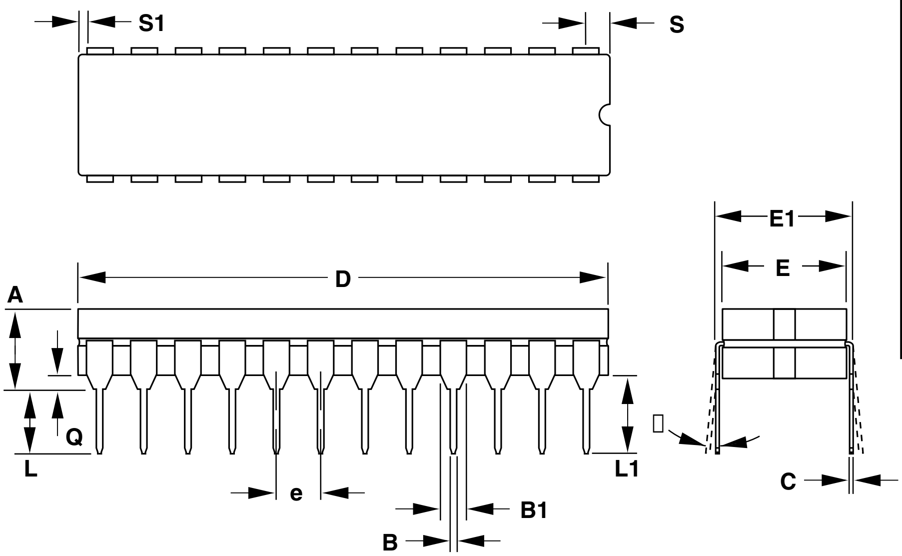
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

21-338A

24-PIN PLASTIC SMALL-OUTLINE PACKAGE

Serial Controlled, 8-Channel SPST Switch

Package Information (continued)



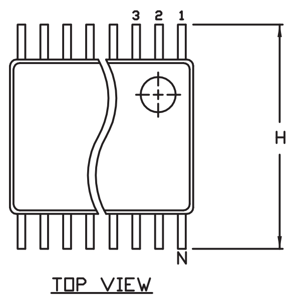
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
D	–	1.280	–	32.51
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.060	0.38	1.52
S	–	0.098	–	2.49
S1	0.005	–	0.13	–
▯	0°	15°	0°	15°

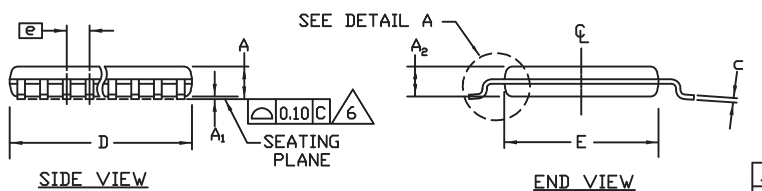
21-340C

24-PIN CERAMIC DUAL-IN-LINE (NARROW) PACKAGE

Serial Controlled, 8-Channel SPST Switch

Package Information (continued)







SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1